

PORTS

10

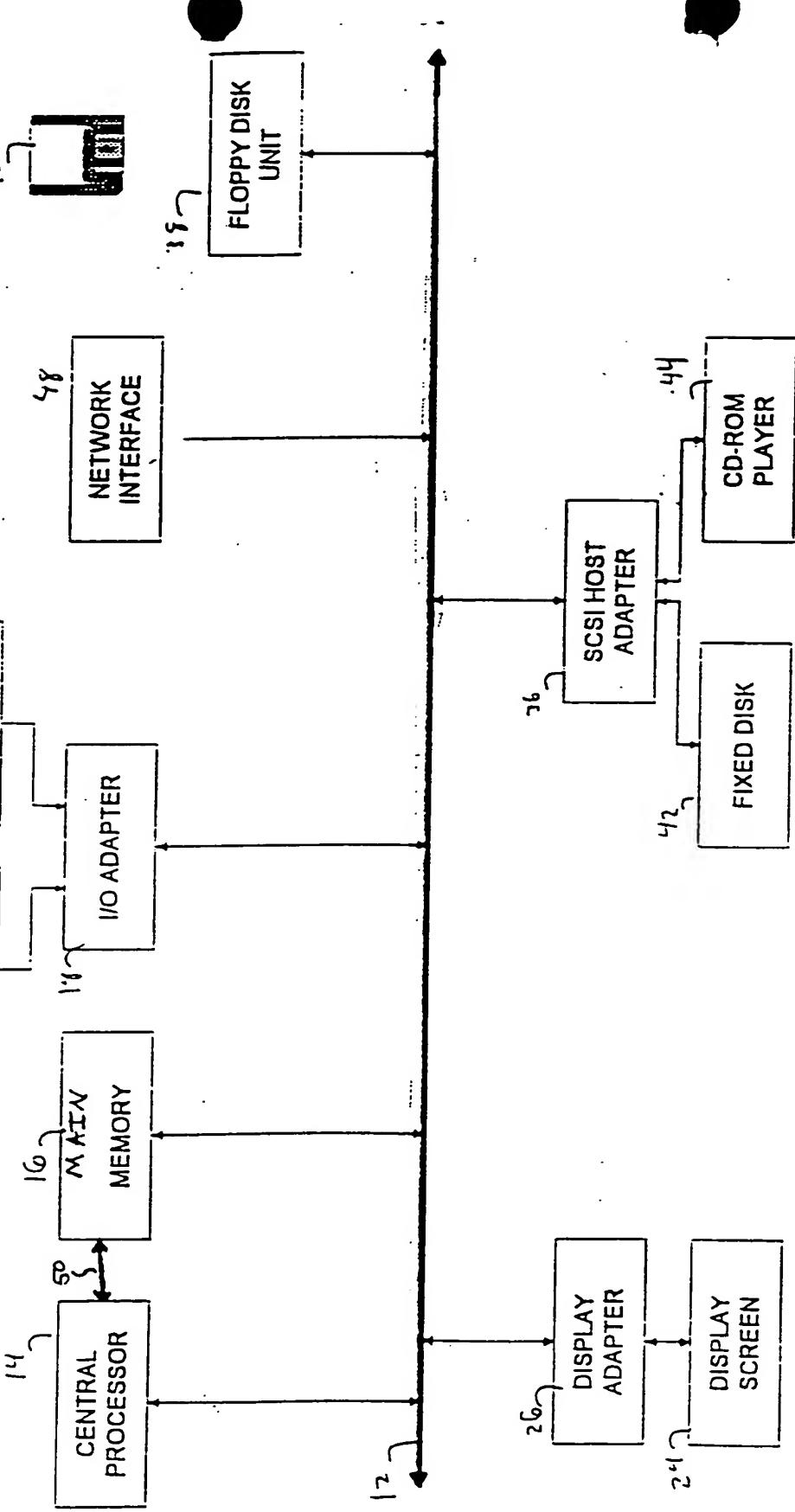
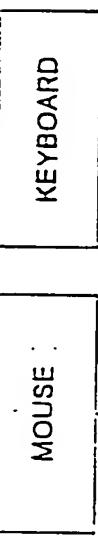


Fig. 1A
(Prior Art)

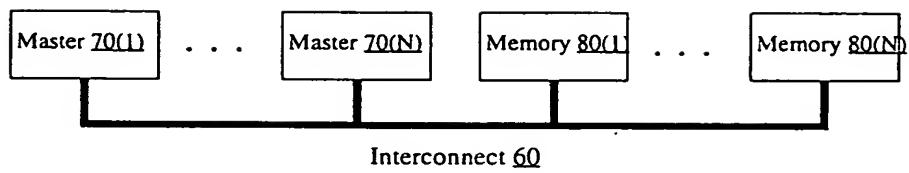


Fig. 1B
(Prior art)

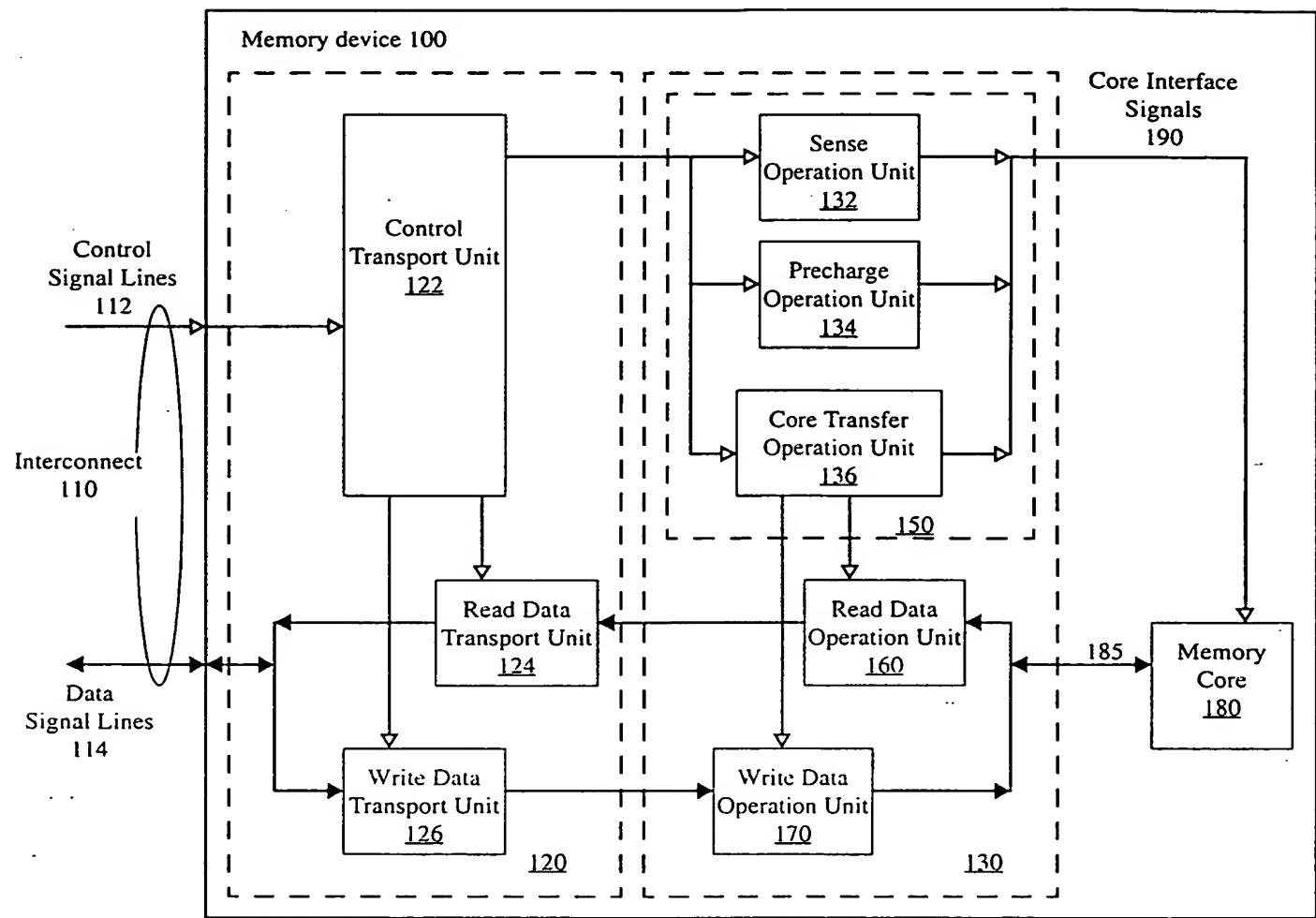


Fig. 1C
(Prior Art)

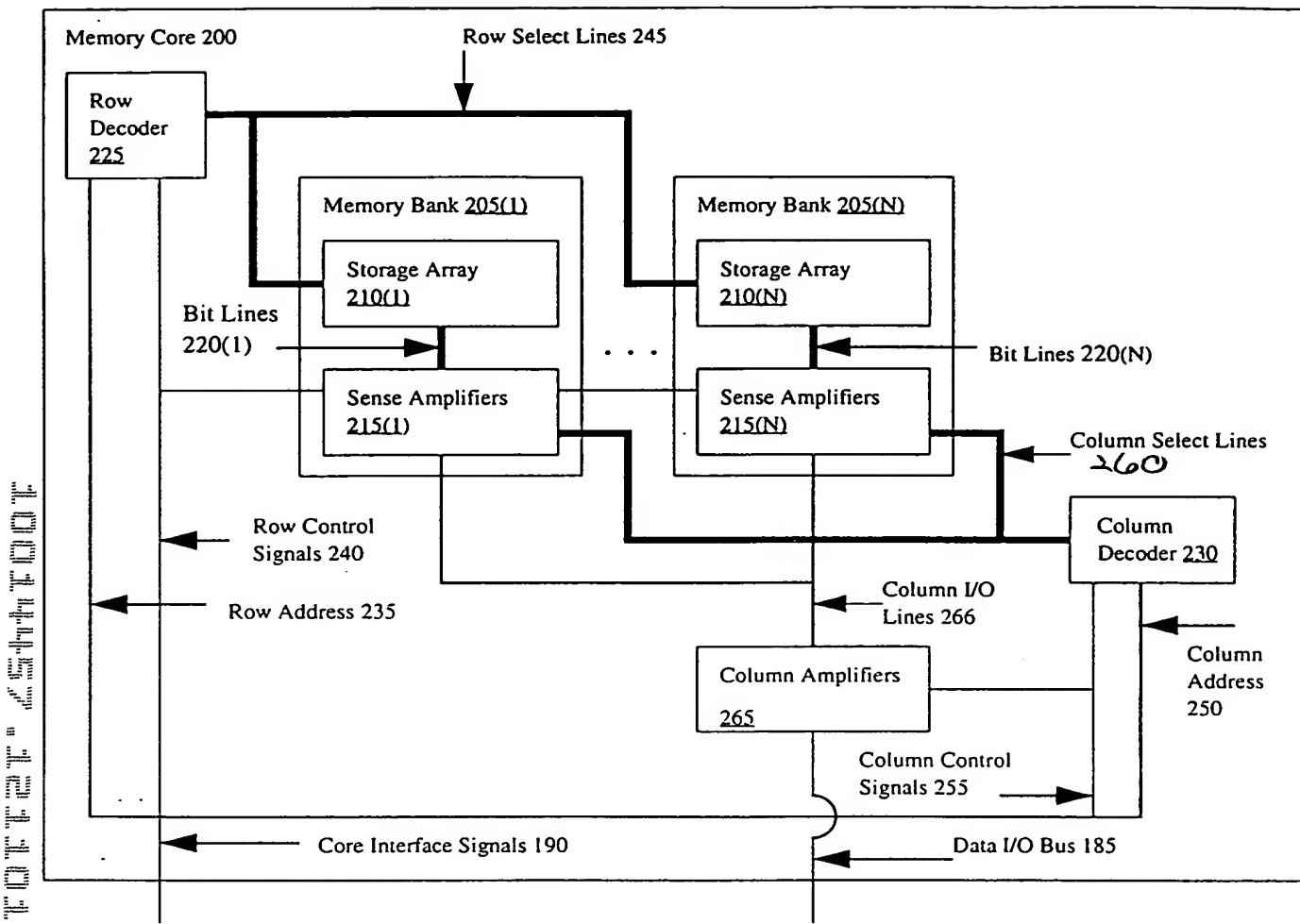


Fig. 2
(Prior Art)

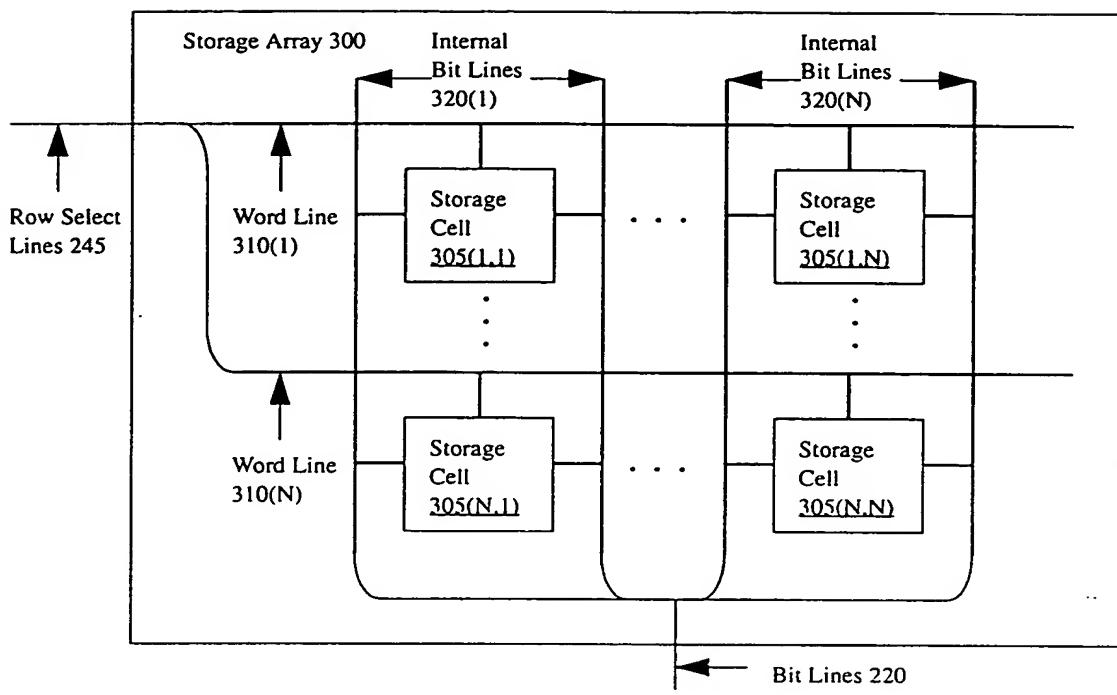


Fig. 3
(Prior Art)

100345 100346 100347 100348

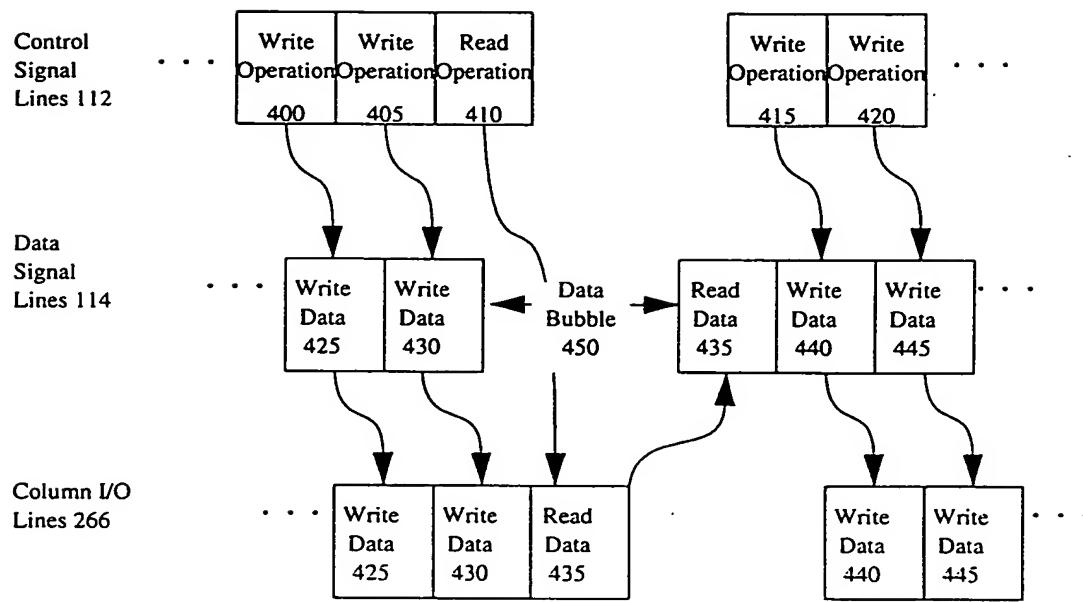


Fig. 4
(Prior Art)

1 0 0 1 1 1 1 1 1 1 1 1 1 1 1

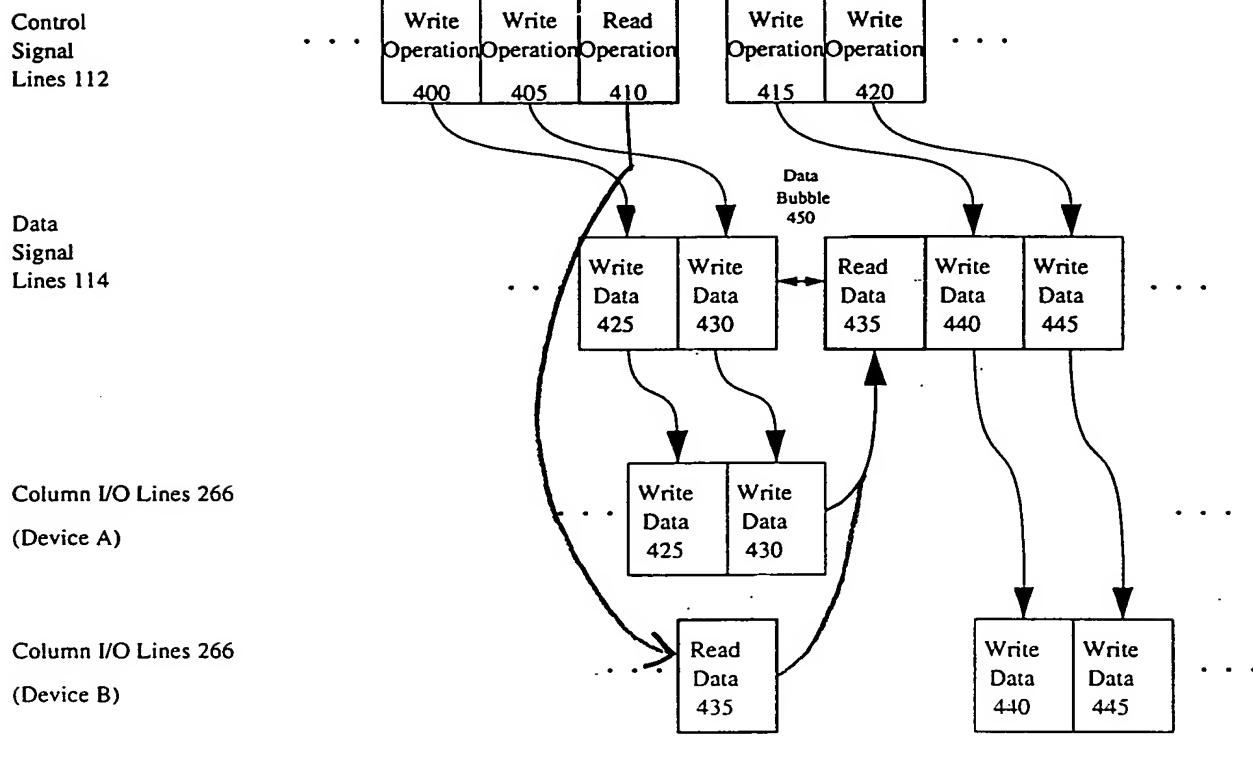


Fig. 5

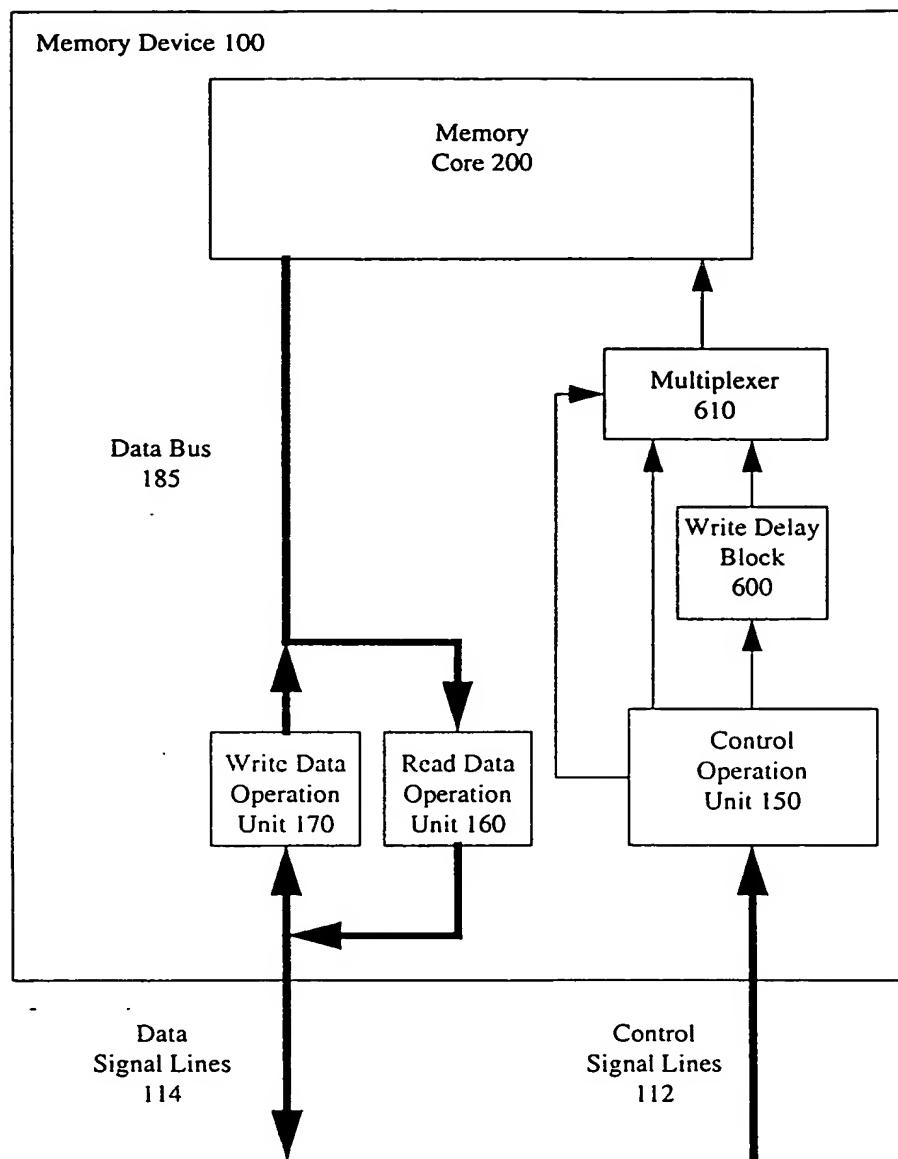


Fig. 6

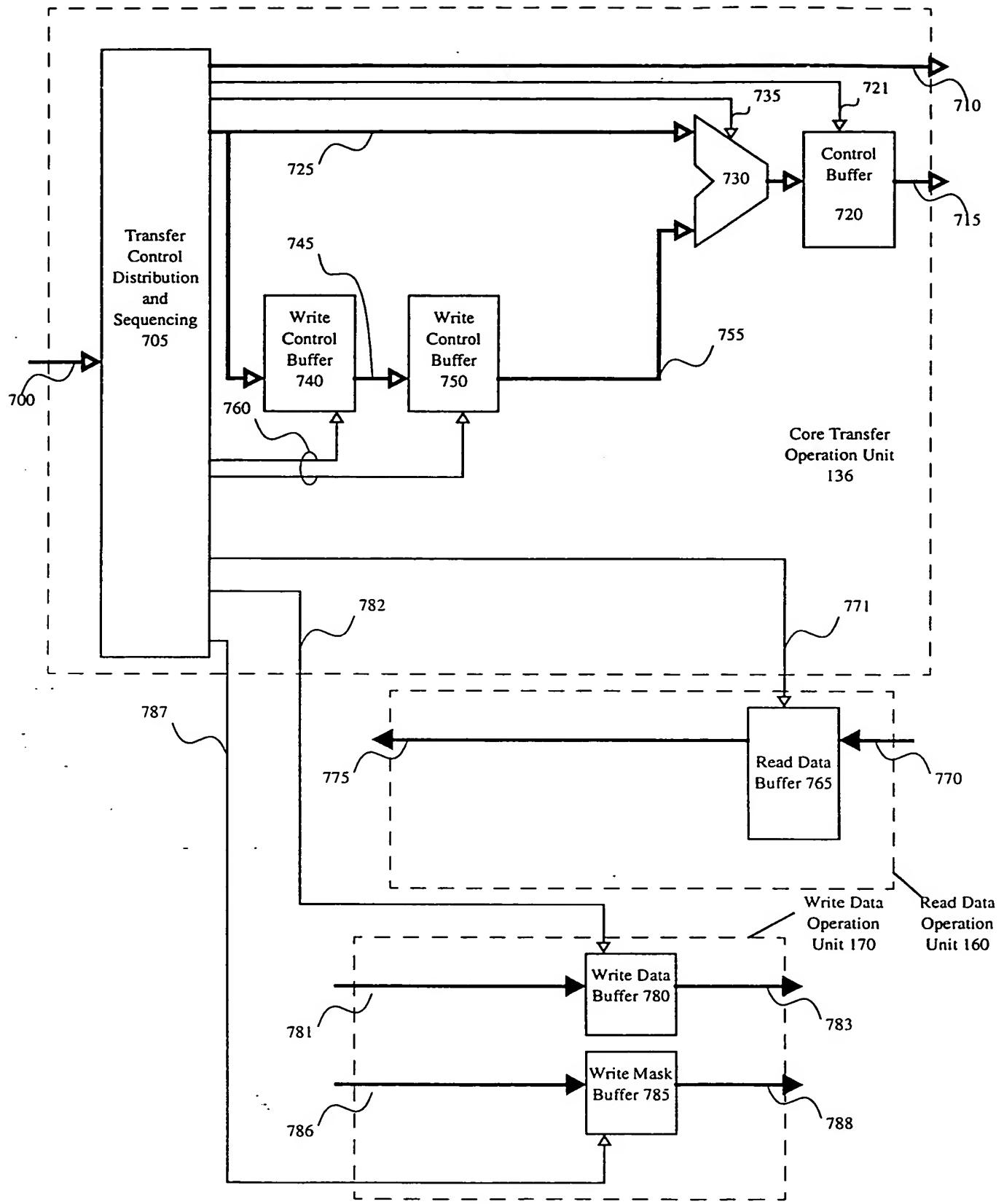


Fig. 7

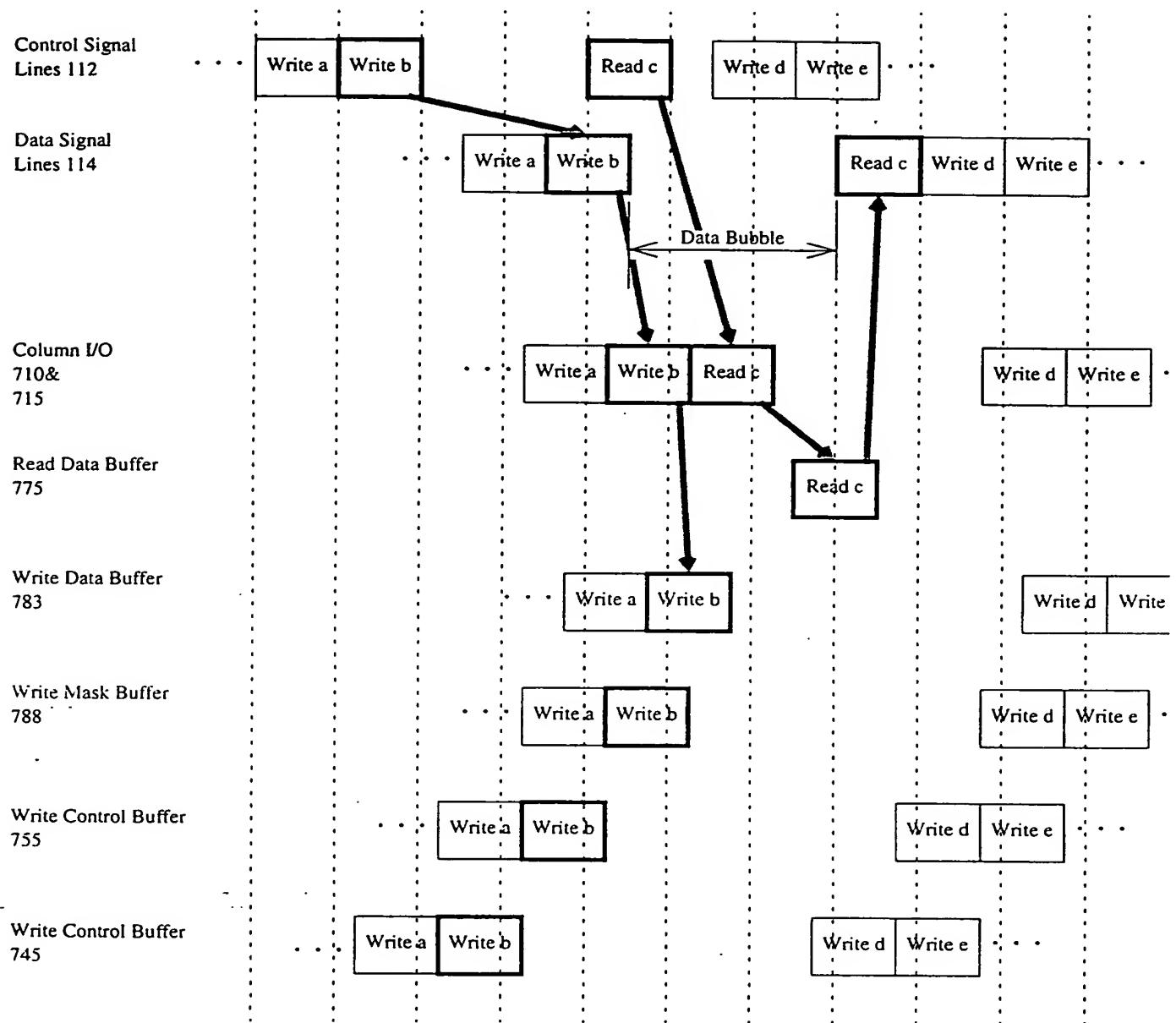


Fig. 8

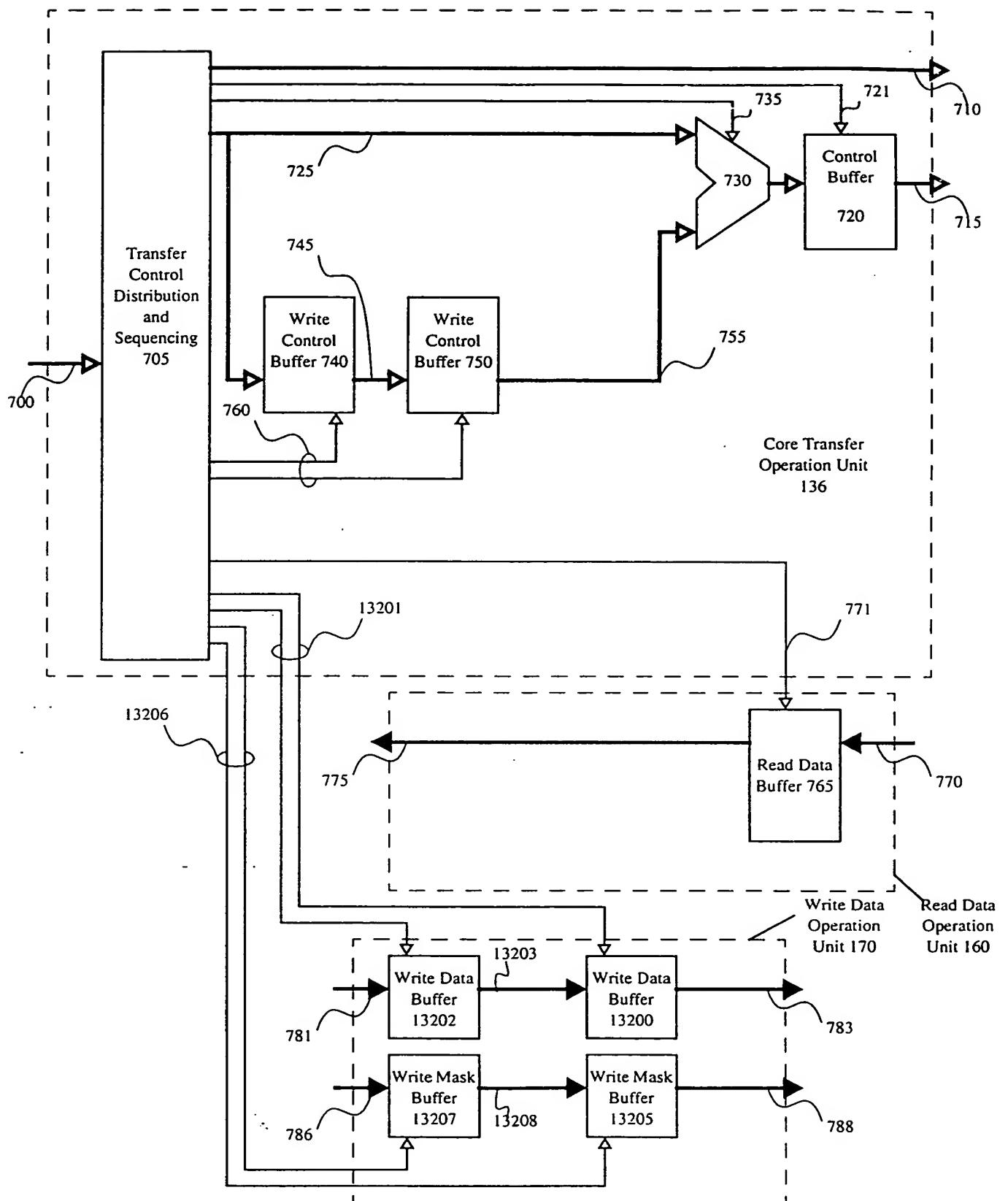
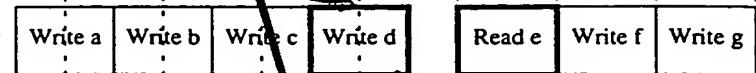


Fig. 9

Control Signal
Lines 112



Data Signal
Lines 114



Column I/O
710&
715



Read Data Buffer
775



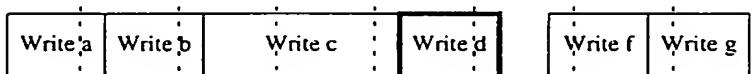
Write Data Buffer
783



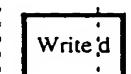
Write Data Buffer
13203



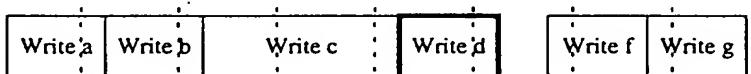
Write Mask Buffer
788



Write Mask Buffer
13208



Write Control Buffer
755



Write Control Buffer
745

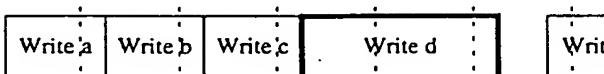


Fig. 10

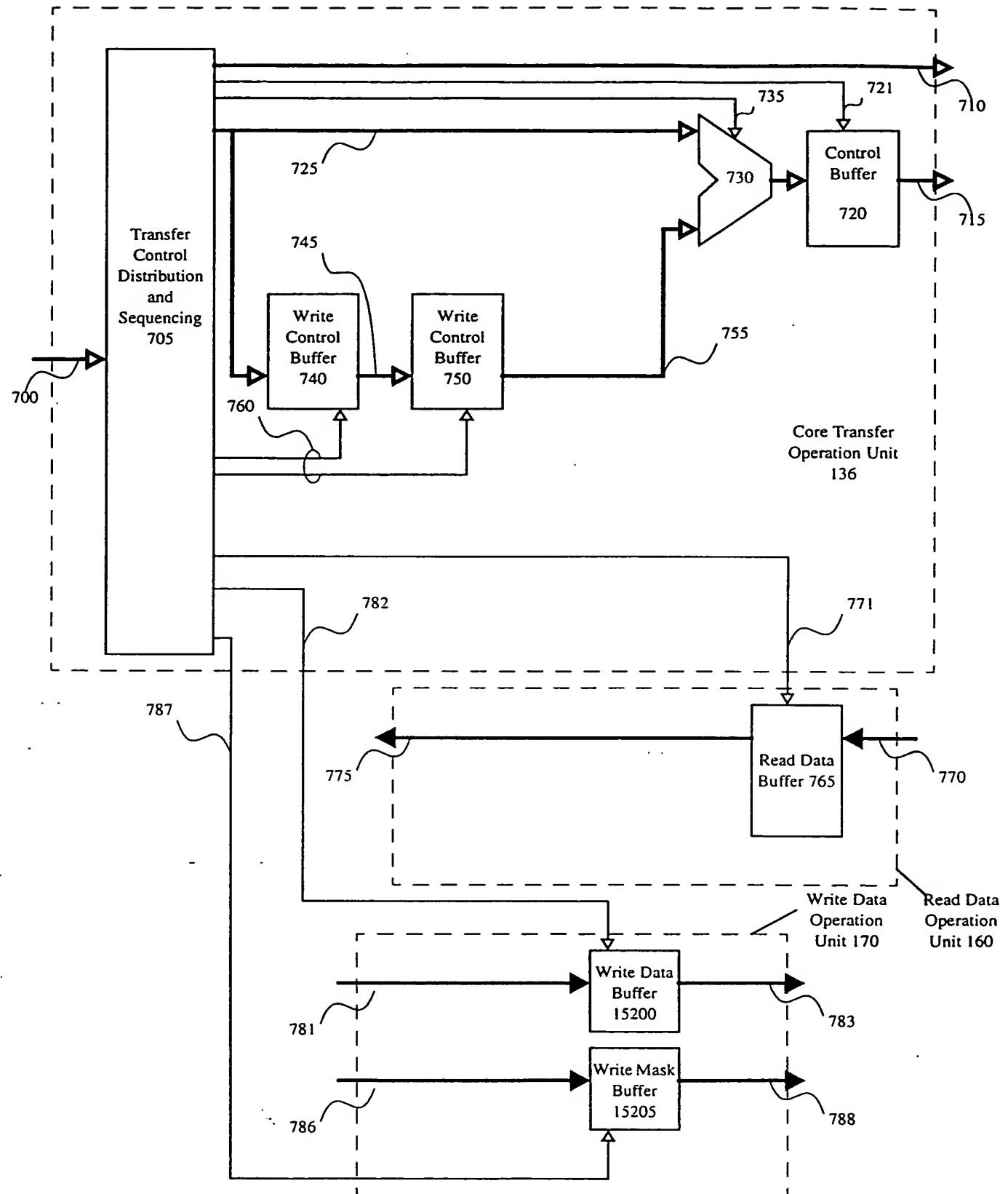


Fig. 11

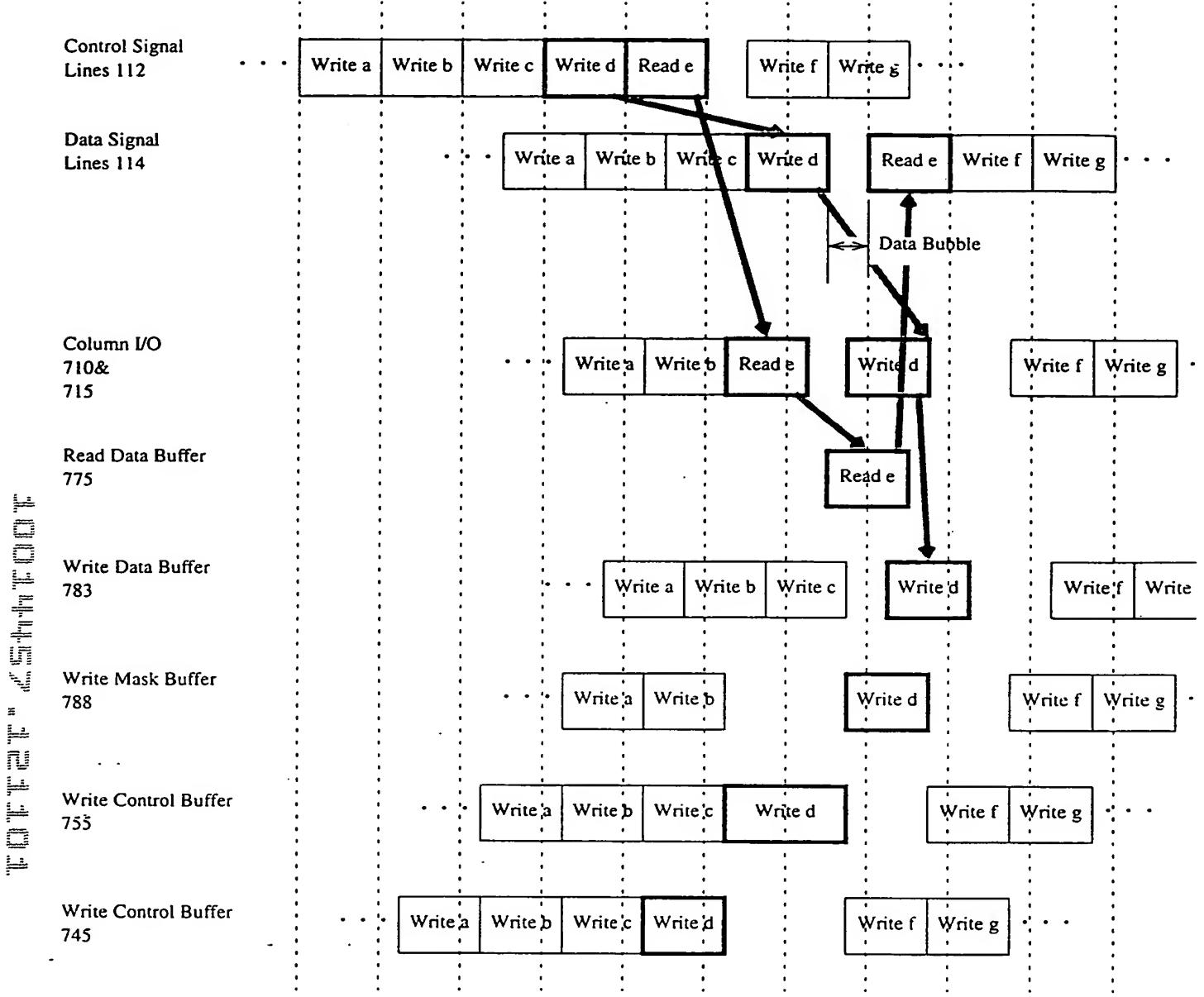


Fig. 12

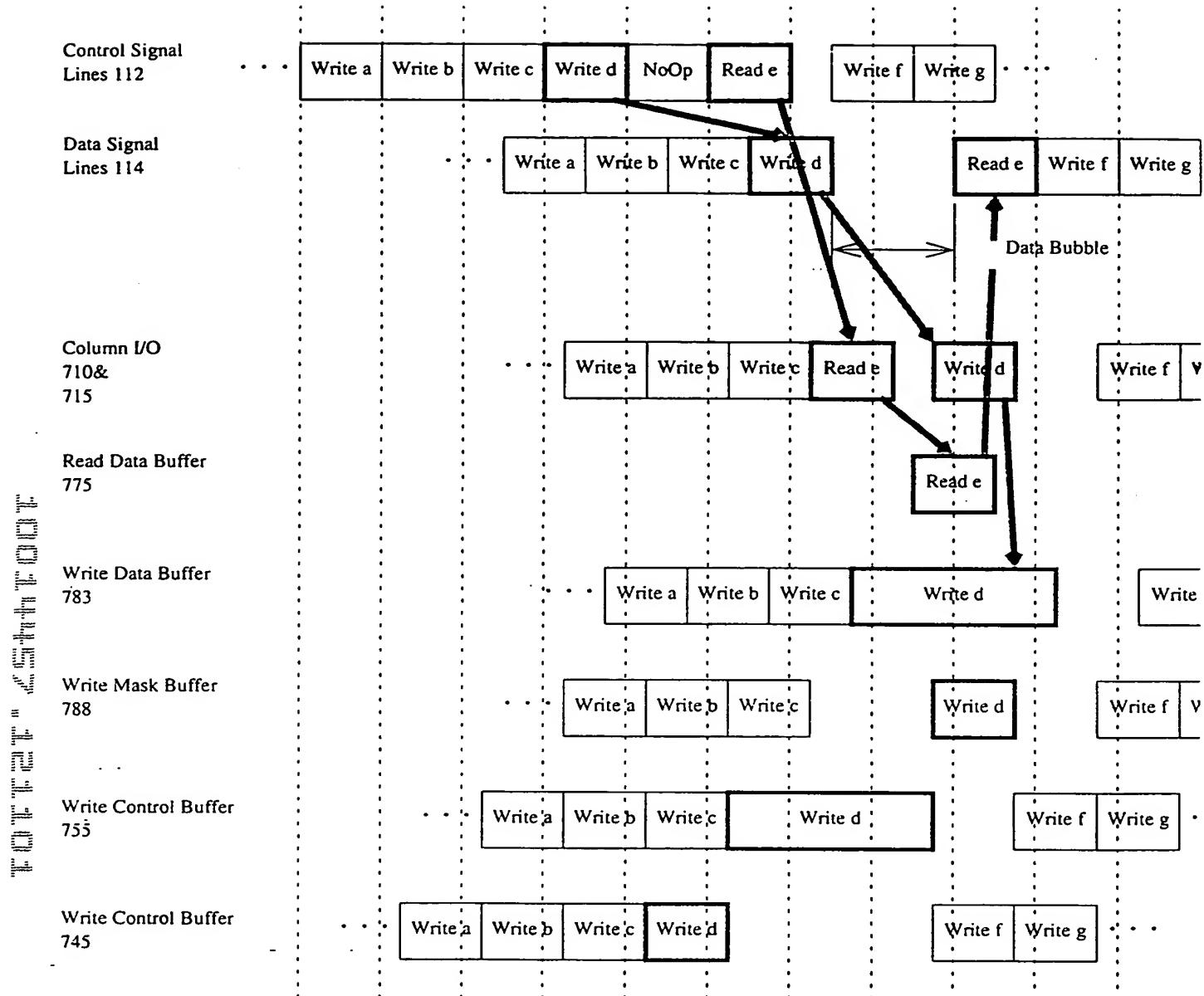


Fig. 13

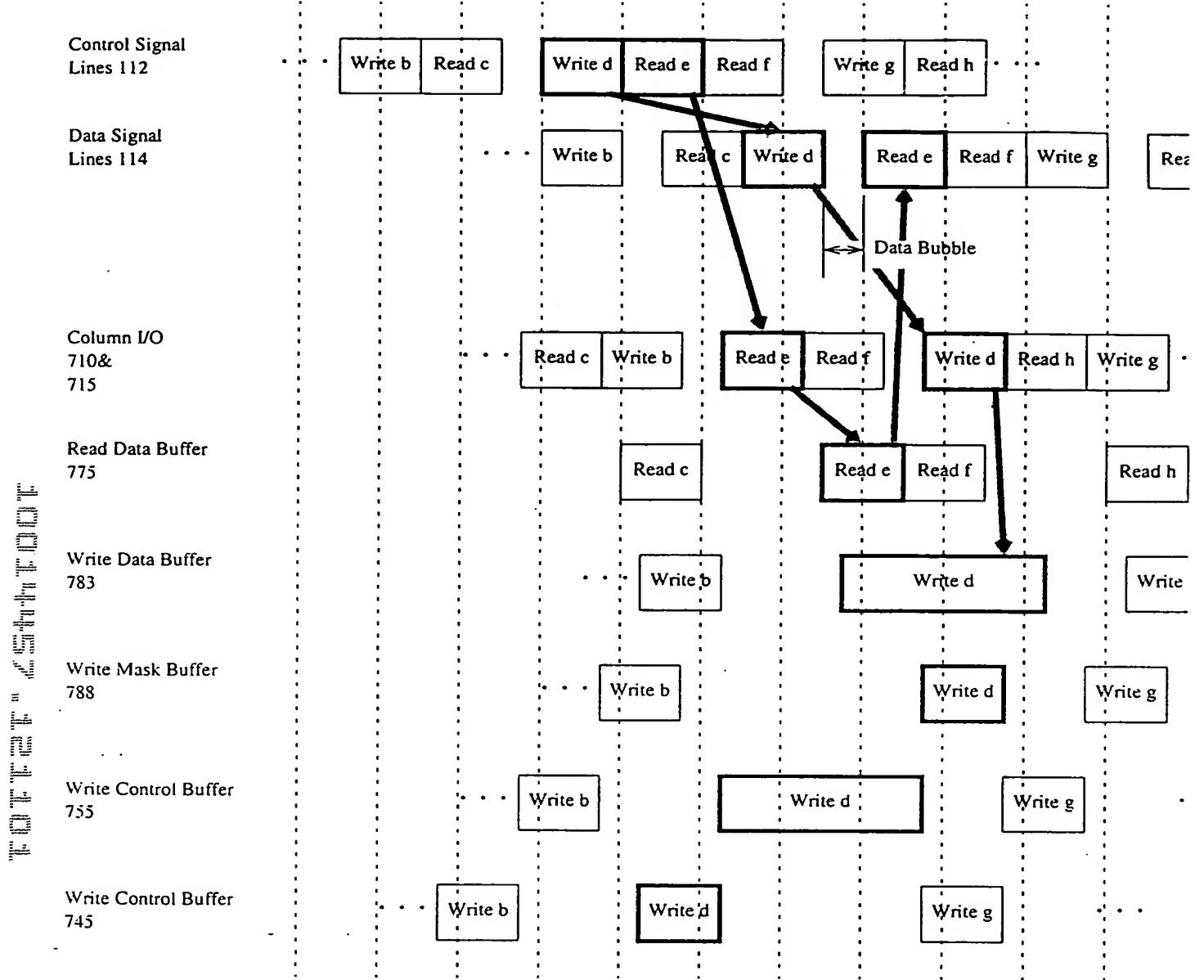


Fig. 14

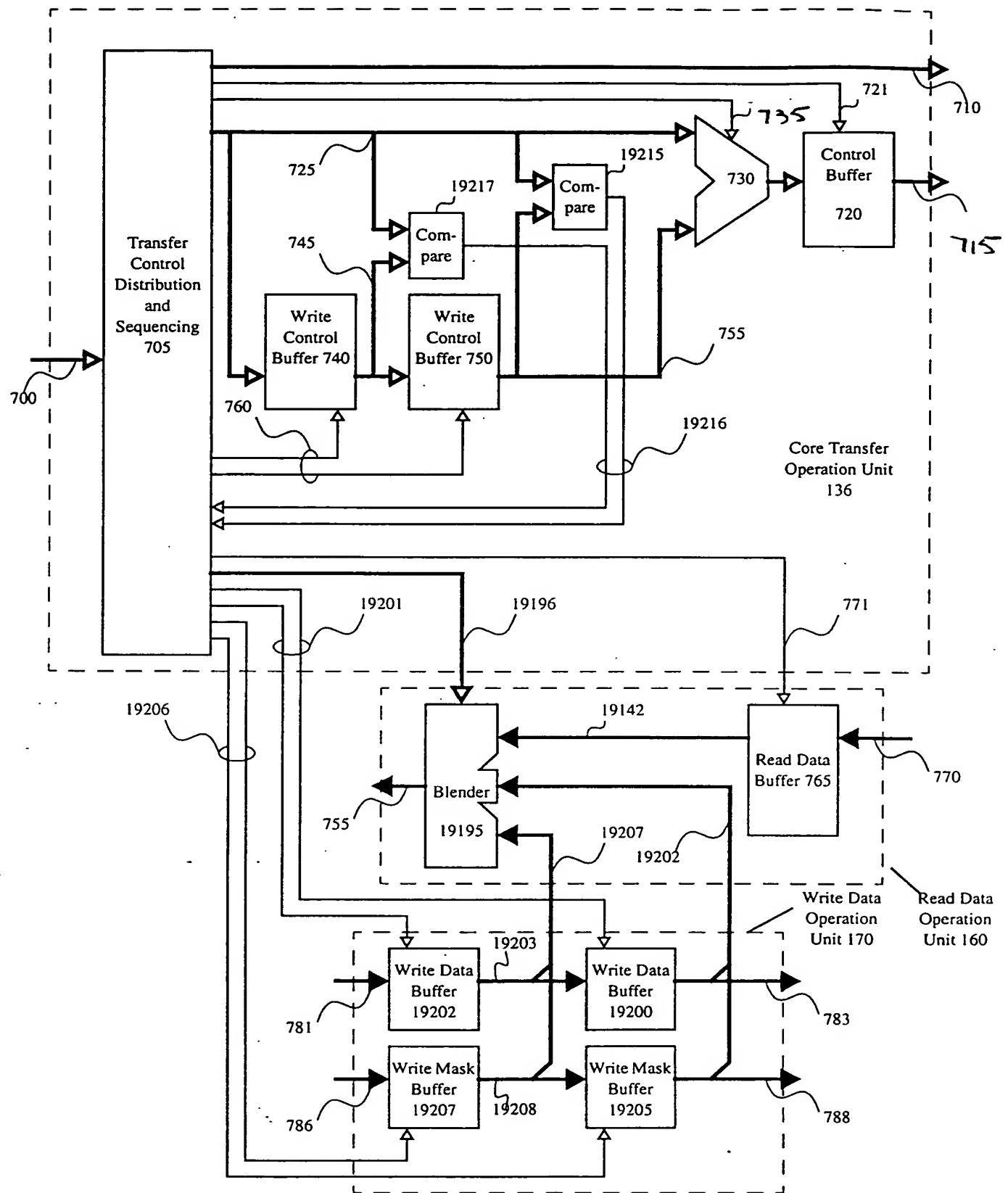


Fig. 15

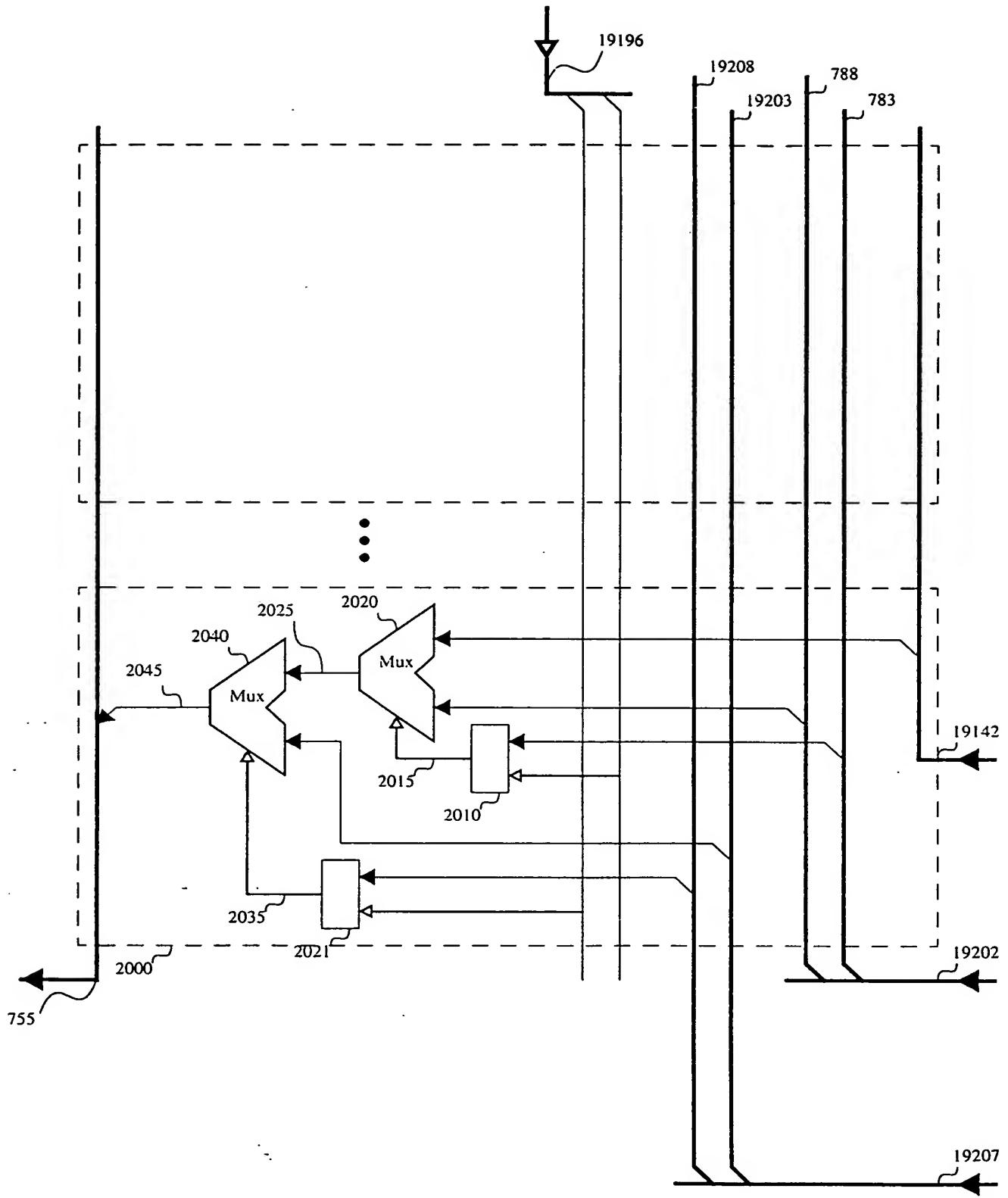


Fig. 16

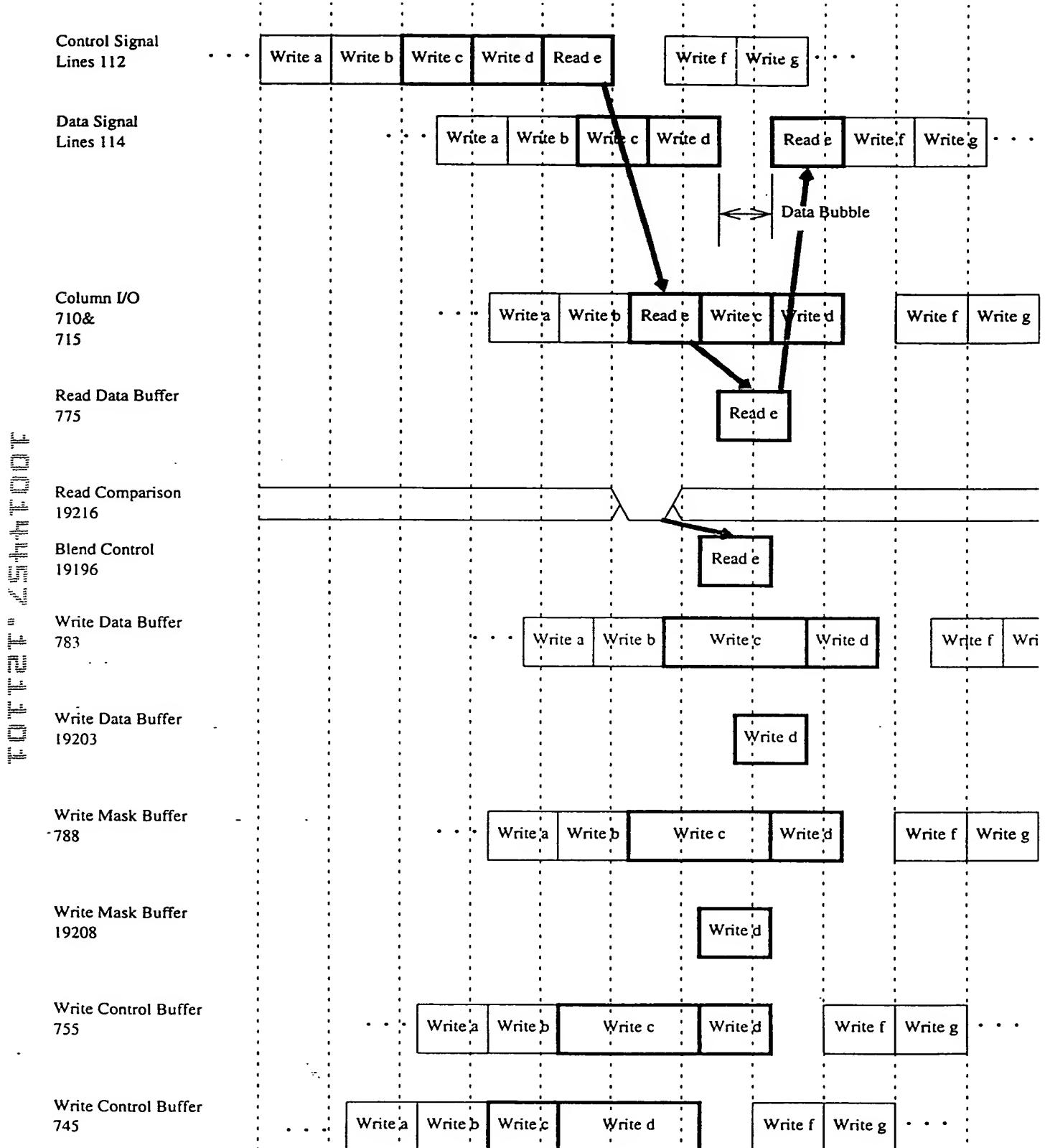


Fig. 17

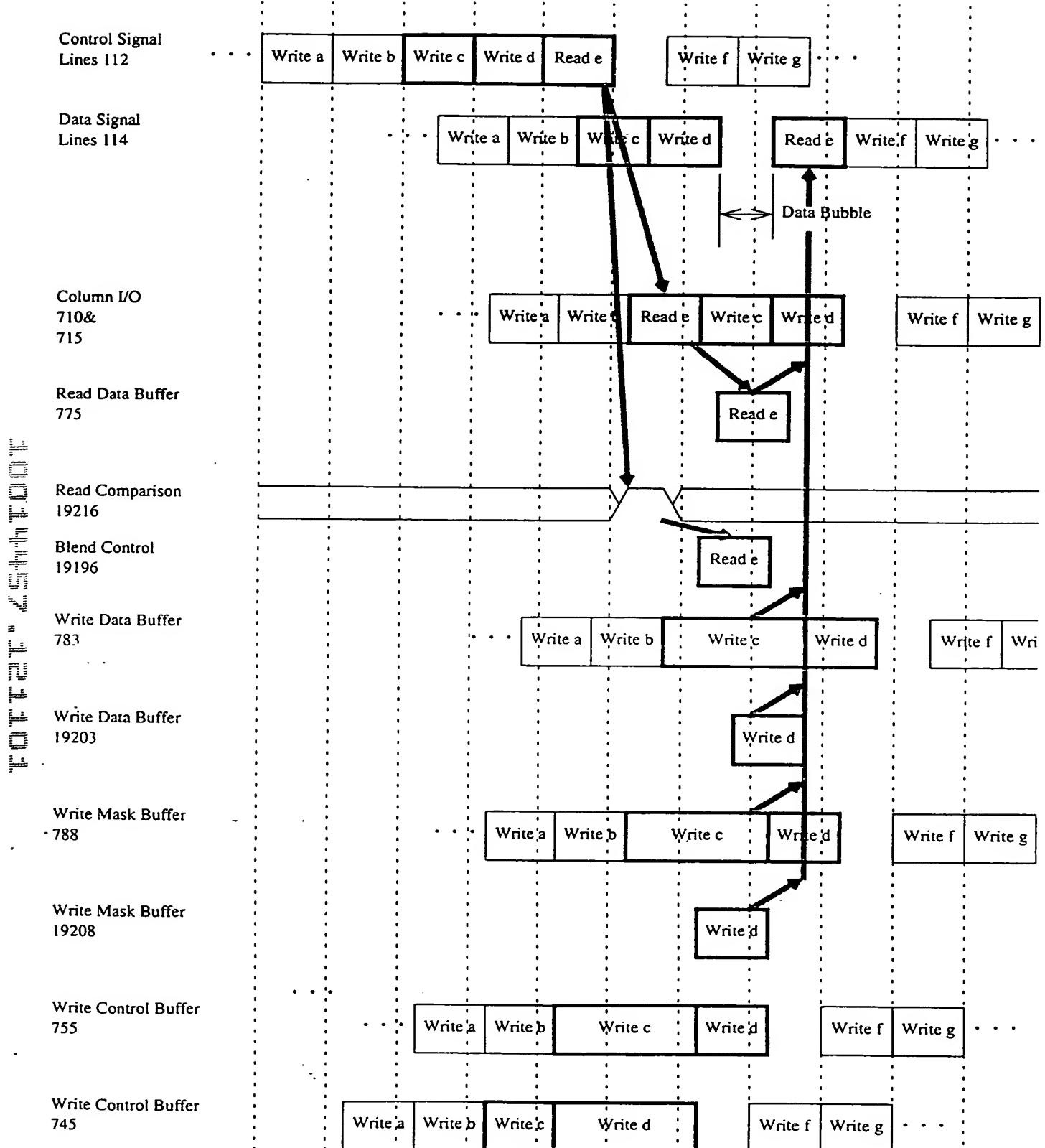


Fig. 18